In the specification:

Please replace the paragraph beginning at page 11, line 19, with the following rewritten paragraph.

--FIG. 8A-8B show a simultaneous lamination process flow according to the invention. Referring to FIG. 8A, laminating layers 802a, 802b, 802c, 802d, and ~~802erespectively~~ 802e respectively having a plurality of vias, conductive patterns and a dielectric layer, a bottom layer 804 and two pad opening layers 806 are aligned and stacked. The pad opening layer 806 could be a dielectric layer or a solder mask. The pad opening layers 806 are optional. FIG. 8B shows the result of simultaneously laminating the laminating layers 802, the bottom layer 804 and the pad opening layers 806 to form a multi-layered substrate. FIG. 8C-8D show another simultaneous lamination process flow according to the invention. Referring to FIG. 8C, laminating layers 808 and 810a, ~~809b, 809c~~ 810b, 810c respectively having a plurality of vias, conductive patterns and a dielectric layer formed by the embodiments mentioned above and a core substrate 812 are aligned and stacked. The core substrate 812 has conductive patterns and several conductive through holes. The layers 808 and 810 can be laminated on one side or both sides of the core substrate 812. FIG. 8D shows the result of simultaneously laminating the laminating layers 808, 810 and the core substrate 812 to form a multi-layered substrate. The layers 808 and 810 can also be laminated with more than one core substrate. In order to improve the bonding between the vias and conductive patterns of two layers, a metal layer 807 can be formed on the vias. The metal layer 807 could comprise solder, nickel gold alloy and a combination of solder and nickel gold alloy.--